Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method comprising:
providing a plurality of pins routed together on a net, wherein each pin has an current value;
calculating a current requirement for each track segment of the net;
determining a track width for each track segment using a current density function; and
performing an automated routing of a first track segment of the net, wherein the automatically routed first track segment has a track width as previously determined using the current density function.

[c2] The method of claim 1 wherein the current density function is provided using a current density table comprising current density as a function of at least one of layer, net frequency, or track width.

[c3] The method of claim 1 further comprising:
providing a frequency of the net and the calculating a current requirement for each track segment of the net takes into account the frequency.

[c4] The method of claim 1 wherein performing an auto-

mated routing of a first track segment of the net comprises using a Steiner tree algorithm.

[c5] The method of claim 1 further comprising:
generating a Steiner tree for the net.

[c6] The method of claim 1
wherein calculating a current requirement for each track segment of the net comprises:
finding a pin of the net with the largest current value and setting as a main driver pin;
setting the largest current value as a current requirement for a second track segment connected to the main driver pin, wherein the second track segment is connected to third and fourth track segments at one point; and
setting a current requirement for a third track segment as a sum of the largest current value and a current requirement for the fourth track segment.

[c7] The method of claim 1 wherein calculating a current requirement for each track segment of the net comprises:
providing a first pin having a first current value connected to a second track segment of the net;
providing a second pin having a second current value connected to a third track segment of the net, wherein the second and third track segments are connected;
setting the first current value as a current requirement

for the second track segment;
setting the second current value as a current requirement for the third track segment;
providing a fourth segment connecting to the second and third track segments; and
setting a sum of the first and second current values as a current requirement for the fourth track segment.

[c8] The method of claim 1 performing an automated routing of a second track segment of the net, wherein the automatically routed second track segment has a track width as previously determined using the current density function, and the track width of the second track segment is different from the track width of the first track segment.

[c9] The method of claim 1 wherein the net is provided in a gridless layout of an integrated circuit design.

[c10] The method of claim 1 wherein the net is provided in a gridded layout of an integrated circuit design.

[c11] The method of claim 1 wherein performing an automated routing of a first track segment of the net comprises:
providing pins of the net;
forming a grid based on positions of the pins;
finding a first route path to connect the pins using the

grid; and

routing around an obstacle in the first route path using an unobstructed path, wherein the unobstructed path is not on the grid.

[c12] The method of claim 11 wherein forming a grid based on positions of the pins occurs after the pins are provided.

[c13] A method comprising:

providing a gridless layout of a circuit design;

providing a plurality of pins of the gridless layout to be routed together using a net;

providing a track width for each track segment of the net; and

performing an automated routing of a first track segment of the net in the gridless layout, wherein the automatically routed first track segment has a first track width as provided.

[c14] The method of claim 13 further comprising:

performing an automated routing of a second track segment of the net in the gridless layout, wherein the automatically routed second track segment has a second track width as provided, and the second track width is different from the first track width.

[c15] The method of claim 13 wherein performing an auto-

mated routing of a first track segment comprises:

forming a grid based on positions of the pins;

finding a first route path to connect the pins using the grid; and

routing around an obstacle in the first route path using an unobstructed path, wherein the unobstructed path is not on the grid.

[c16] A method comprising:

providing a plurality of pins of a layout to be routed together using a net;

creating a Steiner tree for the net including a rule to treat a segment of the layout represented as a number terminal connected to each other, wherein these connections cannot be broken during automated routing;

providing a track width for each track segment of the net; and

using the Steiner tree, performing an automated routing of a first track segment of the net in the gridless layout, wherein the automatically routed first track segment has a first track width as provided.

[c17] The method of claim 16

wherein the rule is replaced by a rule that for shaped items, points at the center and around the perimeter where the perimeter intersects a Hanan grid are added.

[c18] The method of claim 16 wherein the rule is replaced by a rule that all points belonging to the same subnet will be connected together, so the automated routing will not attempt to disconnect these points.

[c19] The method of claim 16 wherein the rule is replaced by a rule that for subpins in the same group that are not connected by an arc, the points for each pin will be replaced by a single point at the center of the subpin.

[c20] The method of claim 16 wherein the rule is replaced by a rule that for subpins that are connected by an arc, both pins will be represented as connected by a forced connection.

[c21] The method of claim 16 wherein the rule is replaced by a rule that buried pins are represented by a point outside a blockage where a first legal routing pitch would be.

[c22] The method of claim 16 wherein the rule is replaced by a rule that a MOS transistor is modeled where its gate is single pin.